

ABSTRACT OF THE THESIS

A PARALLEL SWITCH-LEVEL SIMULATION ALGORITHM

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In this work we develop a new parallel algorithm for switch-level simulation on a general purpose parallel multiprocessor based on a *fully distributed* algorithm called the *Dynamically Directed Switch* (DDS) algorithm. The switch-level model is an abstraction which is used to describe and verify the logical behavior of digital circuits implemented in *Metal Oxide Semiconductor* (MOS) technology. A *graph* of the digital network is formed by the set of electrical nodes (vertices) connected by transistor *switches* (edges). The node values are limited to the values of 0, 1 or X (for intermediate voltages or unknown logic level). All switches are *bidirectional*, which is the main point of difference between the switch-level model and the logic gate-level model. This enables the modeling of charge sharing, pass transistor logic and other configurations which cannot be represented accurately at the gate level. Due to the bidirectional flow of signals, switch-level algorithms typically solve subnetworks collectively, which has been a major stumbling block in the parallelization of such algorithms. In the distributed algorithm, switches and nodes only examine their neighbors to determine their states. To avoid uncontrolled iteration, the instantaneous signal flow of a transistor is used as a state variable, which is shown to be sufficient to guarantee correct results. We demonstrate that the dynamic updating process can be performed in parallel to achieve the maximum degree of parallelism inherent in the circuit. A parallel switch-level simulation system called **PARSL** (PARallel Switch-Level), as implemented on the BBN Butterfly machine, is described and its execution speedup is presented.